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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Cross-talk cancellation scheme for rll-based storage systems

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DESCRIPTION

Field of the invention

The present invention deals with a cross-talk cancellation method, a computer program for implementing a cross-talk cancellation method, a signal processor comprising cross-talk cancellation means, and an apparatus for reading a signal stored along a track on a storage medium, said apparatus comprising cross-talk cancellation means.

The present invention applies to storage systems in which data are stored along tracks on a storage medium. In modern storage systems, the inter-track spacing is chosen relatively small to allow for high storage densities. As a result, when reading a target track, data written on side tracks may appear in the recovered signal. This inter-tracks interference is called cross-talk.

The invention is advantageously used in such storage systems to improve the recovered signal by removing the cross-talk. For instance the invention applies to optical storage systems (DVD, Blu-ray Disc, Small Form Factor Optical Disc...), magnetic storage systems (hard disks notably), magneto-optical storage systems.

With optical storage systems, the cross-talk is even more severe when radial tilt is present in the system because then the optical spot extends more onto the side tracks.

Background of the invention

A cross-talk removing device is described in the US patent 6,134,211. This device has three reading elements simultaneously reading a main track and two adjacent tracks. The three signals that are read by the three reading elements are sampled so as to provide three sequences of samples. A cross-talk removing circuit applies adaptive signal processing (for instance an LMS adaptive algorithm) to the three sequences of samples to produce a cross-talk removed sequence of samples associated to the main track that is free of cross-talk components from the adjacent tracks.

The adaptive processing comprises an adaptive filtering, the filter coefficients being updated so as to converge to zero an error value present in the cross-talk removed sequence of samples.

This convergence is achieved by using a reference sample extracting circuit. When the values of three successive samples transit from positive to negative or from negative to positive, the reference sample extracting circuit extracts the central sample value of three successive sample values. The extracted sample value is supplied to a subtractor that calculates the difference between the extracted sample value and a reference value. This difference is used as the error (e) that has to be converged to zero to update the filter coefficients.

In this scheme it is assumed that the central sample value is the sample value at ideal zero-crossing time. This assumption can only be made if the samples are bit-synchronous samples.

In US 6,134,211 this is achieved by running the analogue to digital converters and the cross-talk removing circuit on a clock that is driven by a time recovery circuit. As a consequence, the cross-talk cancelling scheme is only operational when the time recovery circuit has acquired both the frequency and the phase lock.

In US 6,134,211 when the sample sequences remain in an asynchronous state (that is, when the time recovery circuit is not locked) the sequences are filtered on the basis of fixed predetermined coefficients. This helps to avoid divergence of the filter coefficients but leads to a ramp-up problem: if the time recovery circuit cannot converge because of strong cross-talk, the cross-talk cancellation scheme will remain inefficient and the system will be stuck.

Another problem of the prior art system is that it is hardly compatible with asynchronous receiver architectures.

In such asynchronous architectures, the analogue to digital converters and the filters are run on a fixed clock. A transition from the fixed clock domain to the bit-synchronous domain is done at the output of the cross-talk cancellation circuit by means of a sample rate converter controlled by a time recovery circuit. An additional sample rate controller, locked to the time recovery circuit, would be needed for each adjacent track to produce the bit-synchronous samples that are needed to derive the above-described error (e).

Moreover if the fixed clock (at which the filters are running) and the clock driven by the time recovery circuit (at which the filters coefficients are updated) differ substantially from each other, inverse sample rate converters would also be required to interpolate the filter coefficients from the domain of the clock driven by the time recovery circuit to the domain of the fixed clock.

This would lead to an increased complexity of the architecture.

Summary of the invention

One of the objects of the invention is to propose a solution for cross-talk cancellation that solves the above-mentioned problems.

This is achieved with a cross-talk cancellation method as claimed in claim 1, a program as claimed in claim 2, a signal processor comprising cross-talk cancellation means as claimed in claims 3 to 5, and an apparatus for reading a signal stored along a track on a storage medium as claimed in claims 6 to 8.

The cross-talk cancellation means according to the invention are intended for receiving a main signal associated to a target track and satellite signals associated to side tracks, said main signal showing transitions and runs of various lengths between two transitions. They comprise:

- filtering means for filtering the satellite signals with adaptive filters thereby generating filtered versions of the satellite signals,
- updating means for updating the coefficients of the adaptive filters by minimizing the mismatch between the actual and the expected run length between two transitions of the main signal,

- processing means for generating an improved main signal from said main signal by subtraction of said filtered versions of the satellite signals.

According to the invention the error that is to be minimized when updating the filters coefficients is the mismatch between the actual and the expected run length between two transitions of the main signal. Contrary to the prior art minimization scheme, the minimization scheme of the invention doesn't use the notion of ideal transition time. Therefore it doesn't require the use of bit-synchronous samples. The proposed minimization scheme requires frequency lock but not phase lock.

A first advantage of the proposed minimization scheme is that it resolves the above-mentioned ramp-up problem.

A second advantage of the proposed minimization scheme is that it can be implemented in an asynchronous architecture without any additional hardware complexity.

Advantageously, when used in an asynchronous receiver having a bit clock that is driven by a time recovery circuit, the cross-talk cancellation means of the invention are operated at a fixed clock that is asynchronous with respect to this bit-clock.

In such a case, if the bit clock frequency is different from the fixed clock frequency, additional time recovery means are provided to derive the ratio between the bit clock frequency and the fixed clock frequency, said ratio being used by said updating means for updating said coefficients.

Brief description of the drawings

These and other aspects of the invention will be further described with reference to the following drawings:

- figure 1 and 2 are functional block diagrams of examples of apparatus according to the invention for reading storage medium;
- figures 3 and 4 are schematic representations of a first and a second configuration of tracks and light spots used in a 3-spots cross-talk cancellation scheme;
- figure 5 is a functional block diagram of the cross-talk cancellation means according to the invention;
- figure 6 is a schematic representation of a received signal showing two transitions and a run between the two transitions.

Description of preferred embodiments

The invention applies to storage media having tracks forming each a 360° turn of a spiral line. Encoded data are recorded along the tracks. The encoding scheme that is used in optical recording system is a Run Length Limited encoding scheme (RLL). When the data recorded along the tracks are encoded with an RLL encoding scheme, the tracks exhibit marks corresponding to runs of a same value, and the edges of a mark correspond to a transition

between two runs. The size of the mark corresponds to the length of the run. It is an integer multiple of a reference unit size mark.

Figures 1 and 2 shows block diagrams of a first and a second example of apparatus for reading such a disc. The apparatus described in figure 1 caries reference number 6-1. The apparatus of figure 2 caries reference number 6-2. According to figures 1 and 2, the apparatus 6-1 and 6-2 comprise an optical unit 8 having three reading elements: a main reading element 12 for reading a main signal associated to a main track, and two satellite reading elements 11 and 13 for reading two satellite signals associated to the two tracks that are adjacent to the main track. In the following of the description one of these satellite signal is called upper satellite signal, and the other satellite signal is called lower satellite signal. The three reading elements transmit three light spots 21, 22 and 23.

Figures 3 and 4 show the location of the three light spots 21, 22 and 23 with respect to the three tracks to be read 31, 32 and 33. The main light spot 22 is centred on the main track 32. The satellite light spots 21 and 23 can be centred either on the satellite tracks 31 and 33 as represented in figure 3, or between the main track 32 and the adjacent tracks 31 and 33 as represented in figure 4. The satellite signals read by the satellite light spots 21 and 23 in figures 3 and 4 are said to be "associated to" the adjacent tracks because the light spots 21 and 23 overlay with at least part of the adjacent tracks.

The embodiment of figure 4 is advantageous for rewritable optical disc systems because it allows reusing the 3-spots push-pull radial tracking means which are currently available in all such systems (the signal read by the reading elements 11, 12 and 13 and the main light spots 21, 22 and 23 can be used both for tracking and for cross-talk cancellation).

Coming back to figures 1 and 2, the three signals that are read by the three reading elements 11, 12 and 13 are input to a signal processor 40 comprising cross-talk cancellation means 42 and decoding means 44. The signal produced by the decoding means 44 is input to a reproduction circuit 46 that generates an output signal (for instance an audio or a video signal).

Figure 5 is a functional representation of the cross-talk cancellation means 42. The cross-talk cancellation means 42 comprise three analogue-to-digital converters 51, 52 and 53 for sampling the main signal, the upper satellite signal and the lower satellite signal. The three analogue-to-digital converters 51, 52 and 53 operate at a fixed clock 55 and generate a sequence of main samples 62, a sequence of lower satellite samples 61, and a sequence of upper satellite samples 63. The sequences of lower and upper satellite samples 61 and 63 are respectively processed by a lower adaptive filter 71 and an upper adaptive filter 73 which respectively generate a filtered version 81 of the sequence of lower satellite samples and a filtered version 83 of the sequence of upper satellite samples. The sequence 62 of main samples is processed by an optional equalizer 90 which generates an equalized sequence of main samples 92. Then a subtractor 93 subtracts the filtered version 81 of the sequence of lower satellite samples and a filtered version 83 of the sequence of upper satellite samples from the

equalized sequence 92 of main samples thereby generating an improved sequence of main samples 102.

Alternatively, when the equalizer 90 is omitted, the improved sequence of main samples 102 is generated by subtracts the filtered version 81 of the sequence of lower satellite samples and a filtered version 83 of the sequence of upper satellite samples from the sequence 62 of main samples.

The improved sequence of main samples 102 is input to a sample rate converter 120 driven by a time recovery circuit 130 (for instance a Phase Lock Loop circuit). The output of the sample rate converter 120 is the input of the decoding means 44.

The improved sequence of main samples 102 and the sequences of lower and upper satellite samples 61 and 63 are processed by lower and upper coefficient updating means 111 and 113. The lower and upper coefficient updating means 111 and 113 respectively update the coefficients used by the lower filter 71 and by the upper filter 73.

The behaviour of the cross-talk cancellation means 42 can be formalized y the following mathematical expression:

$$\tilde{C}_m = C_m - \sum_k f_k^+ S_{m-k}^+ - \sum_k f_k^- S_{m-k}^- \qquad \textbf{(equation 1)}$$

where:

S_m^+ is the sample m of the upper satellite signal;

S_m^- is the sample m of the lower satellite signal;

C_m is the sample m of the main signal;

f_k^+ are the coefficients of the upper filter and f_k^- are the coefficients of the lower filter;

$\tilde{C}_m$ is the improved main sample m obtained at the output the subtractor 93.

Advantageously the algorithm used to update the filter coefficients is the LMS algorithm (Least Mean Square). According to the invention the driving term Z_m of the algorithm (that is the term to be minimized) is the mismatch between the actual and the expected run length between two transitions of the main signal.

This means that:

$$\left(f_k^{\pm}\right)_{m+1} = (1-\mu)\left(f_k^{\pm}\right)_m - \mu \frac{\partial}{\partial f_k^{\pm}} (Z_m)^2 \qquad \textbf{(equation 2)}$$

The cross-talk minimization scheme of the invention will be described below by reference to figure 6. As will be apparent from this description, for the proposed scheme to operate properly, the ratio α between the PLL-driven bit clock and the fixed clock that runs the analogue-to-digital converters 51, 52 and 53 must be available. In figure 5 two arrows 141 and 143 indicate that the frequency ratio α is supplied to the first and second coefficient updating

means 111 and 113. The arrows 141 and 143 are represented in dash lines because they can be omitted when the frequency ratio α is equal to 1.

The ratio α is advantageously supplied by a time recovery circuit external to the cross-talk cancellation means 42 and specifically designed for fast approximate recovery of the bit frequency. Such an external time recovery circuit is already present in most reading apparatus.

For instance in some systems (mostly in writable/rewritable systems), the wobble clock can be conveniently used for estimating the ratio α. Figure 1 gives an example of implementation that will be advantageously used in such systems: in figure 1, the external time recovery circuit carries reference number 50-1 and is connected on the path between the main reading element 12 and the cross-talk cancellation means 42. In other systems (mostly in ROM systems), average run length measurements can be used for the same purpose. Figure 2 gives an example of implementation that will be advantageously used in such systems: in figure 2, the external time recovery circuit carries reference number 50-2 and is connected on the path between the cross-talk cancellation means 42 and the decoding means 44.

Figure 5 is a schematic representation of the received main signal. Two successive transitions X_m and X_{m+1} are represented.

$\tilde{C}_{(m,L)}$ is the improved main sample at the left of the transition X_m;

$\tilde{C}_{(m,R)}$ is the improved main sample at the right of the transition X_m;

$\tilde{C}_{(m+1,L)}$ is the improved main sample at the left of the transition X_{m+1};

$\tilde{C}_{(m+1,R)}$ is the improved main sample at the right of the transition X_{m+1};

$\tilde{C}_{(m,L)-1}$ is the improved main sample that precedes sample $\tilde{C}_{(m,L)}$;

$\tilde{C}_{(m,L)+1}$ is the improved main sample that follows sample $\tilde{C}_{(m,L)}$;

$\tilde{C}_{(m,R)-1}$ is the improved main sample that precedes sample $\tilde{C}_{(m,R)}$;

$\tilde{C}_{(m,R)+1}$ is the improved main sample that follows sample $\tilde{C}_{(m,R)}$;

φ_m is the time interval between the ideal time of the transition X_m and the actual time of the transition X_m (in figure 5, $\varphi_m < 0$);

φ_{m+1} is the time interval between the ideal time of the transition X_{m+1} and the actual time of the transition X_{m+1} (in figure 5, $\varphi_{m+1} < 0$);

$d_{m+1,m}$ is the actual run length between the two transitions X_m and X_{m+1}.

In the following for simplification purposes it is assumed, without loss of generality, that:

- the time interval between two samples is equal to 1,

- the transition moment m=1 corresponds to a raising transition,

- and the time interval φ_m takes values from the interval $\left[-\frac{1}{2},+\frac{1}{2}\right]$.

A first implementation of the updating scheme of the invention will now be described. This first implementation is applicable when the fixed system clock is (nearly) equal to the PLL driven bit clock (that is when the ratio α is close to 1) but there is no phase lock between the two clocks.

The LMS driving parameter to be minimized Z_m is chosen equal to the difference between the actual run length $d_{m+1,m}$ and the expected run length $d^{(\exp)}_{m+1,m}$. Taking into account that an integer number of clock intervals should ideally fit between the transitions in the RLL encoded signal when there is no inter-symbol interference and no clock frequency variations, $d^{(\exp)}_{m+1,m}$ can be approximated as $d^{(\exp)}_{m+1,m}=round\left(d_{m+1,m}\right)$ where $round(x)$ is defined as the integer number that is the closest to the real number x.

Thus $Z_m=\zeta(d_{m+1,m})$ where $\zeta(x)=x-round(x)$ **(equation 3)**

with $d_{m+1,m}=[(m+1,L)-(m,L)]+\varphi_{m+1}-\varphi_m$

where $[(m+1,L)-(m,L)]$ denotes the integer number of sampling intervals between the samples $\tilde{C}_{(m,L)}$ and $\tilde{C}_{(m+1,L)}$.

In the following it is assumed that the cross-talk is not extremely large so that for small variations of the filter coefficients $\left|\zeta\left(d_{m+1,m}\right)\right|<\frac{1}{2}$.

With this assumption, Z_m can be approximated as follows:

$Z_m=\zeta\left(d_{m+1,m}\right)\approx\varphi_{m+1}-\varphi_m+E$ where E is an integer independent of the filter coefficients.

$$\Rightarrow\frac{\partial Z_m}{\partial f_k^{\pm}}=\frac{\partial(\varphi_{m+1}-\varphi_m)}{\partial f_k^{\pm}} \qquad \textbf{(equation 4)}$$

The time interval φ_m can be computed approximately as a function g_m of the improved main samples:

$$\varphi_m\approx g_m\left(\tilde{C}_{(m,L)},\tilde{C}_{(m,L)-1},\ldots,\tilde{C}_{(m,L)-N_L},\tilde{C}_{(m,R)-1},\ldots,\tilde{C}_{(m,R)-N_R}\right)(-1)^m$$

The general form of a linear approximation is:

$$\varphi_m\approx\left(\sum_{k=0}^{N_L}\eta_{k,L}\tilde{C}_{(m,L)-k}+\sum_{k=0}^{N_R}\eta_{k,R}\tilde{C}_{(m,R)-k}\right)(-1)^m$$

A simple 2-terms linear approximation can be used which gives:

$\varphi_m \approx \eta.\left(\tilde{C}_{(m,L)} + \tilde{C}_{(m,R)}\right).(-1)^m$ with $\eta_{k,L} = \eta_{k,R} = \eta > 0$

and $\varphi_{m+1} \approx \eta.\left(\tilde{C}_{(m+1,L)} + \tilde{C}_{(m+1,R)}\right).(-1)^{m+1}$.

Based on this simple 2-terms linear approximation and on equation 3 above:

$$Z_m \approx \zeta\left(\eta R_m.(-1)^{m+1} + [(m+1,L) - (m,L)]\right) = \zeta(\eta R_m).(-1)^{m+1}$$

where $R_m = \tilde{C}_{(m,L)} + \tilde{C}_{(m,R)} + \tilde{C}_{(m+1,L)} + \tilde{C}_{(m+1,R)}$

The term $\frac{\partial}{\partial f_k^{\pm}}(Z_m)^2$ in equation 2 can be computed as follows:

$$\frac{\partial}{\partial f_k^{\pm}}(Z_m)^2 = 2.Z_m.\frac{\partial Z_m}{\partial f_k^{\pm}} \approx 2.\zeta(\eta R_m).(-1)^{m+1}.\frac{\partial(\varphi_{m+1} - \varphi_m)}{\partial f_k^{\pm}}$$

$$\Rightarrow \frac{\partial}{\partial f_k^{\pm}}(Z_m)^2 \approx 2\eta.\zeta(\eta R_m).\left[S^{\pm}_{(m,L)-k} + S^{\pm}_{(m,R)-k} + S^{\pm}_{(m+1,L)-k} + S^{\pm}_{(m+1,R)-k}\right]$$

Eventually the expression for updating the filters coefficients is:

$$\left(f_k^{\pm}\right)_{m+1} = (1-\mu)\left(f_k^{\pm}\right)_m - 2.\mu.\eta.\zeta(\eta R_m).\left(S^{\pm}_{(m,L)-k} + S^{\pm}_{(m,R)-k} + S^{\pm}_{(m+1,L)-k} + S^{\pm}_{(m+1,R)-k}\right)$$

(equation 5)

A second implementation of the updating scheme of the invention will now be described that can be used when the fixed system clock (under which the filters are running) is not equal to the PLL driven bit clock (that is when the ratio $\alpha \neq 1$).

In this second implementation, the LMS driving parameter to be minimized Z_m is also chosen equal to the difference between the actual run length $d_{m+1,m}$ and the expected run length $d^{(\exp)}_{m+1,m}$, but the mathematical formulae used for computing $d_{m+1,m}$, φ_m and φ_{m+1} have to be modified so as to take into account the frequency ratio α.

Namely, in order to measure the run length in bit intervals the number of samples between two transitions has to be multiplied by α which means that:

$$d_{m+1,m} = \alpha.[(m+1,L) - (m,L)] + \varphi_{m+1} - \varphi_m$$

The transitions phase φ_m also have to be multiplied by α. This means that the general form of the linear approximation of φ_m is:

$$\varphi_m \approx \alpha.\left(\sum_{k=0}^{N_L} \eta_{k,L}\tilde{C}_{(m,L)-k} + \sum_{k=0}^{N_R} \eta_{k,R}\tilde{C}_{(m,R)-k}\right)(-1)^m$$

and the simple 2-terms expression of the linear approximation is:

$$\Rightarrow \varphi_m \approx \alpha\eta.\left(\tilde{C}_{(m,L)} + \tilde{C}_{(m,R)}\right).(-1)^m$$

Eventually the expression for updating the filters coefficients is:

$$\left(f_k^{\pm}\right)_{m+1} = (1-\mu)\left(f_k^{\pm}\right)_m - 2.\alpha.\mu.\eta.\zeta(\eta R_m)\left[S^{\pm}_{(m,L)-k} + S^{\pm}_{(m,R)-k} + S^{\pm}_{(m+1,L)-k} + S^{\pm}_{(m+1,R)-k}\right]$$

(equation 6)

It will be noted from equations 5 and 6 that the minimization scheme of the invention doesn't use the notion of ideal transition time.

With respect to the described cross-talk cancellation method, signal processor and reading apparatus, modifications or improvements may be proposed without departing from the scope of the invention. The invention is not limited to the examples provided. In particular:

- The first and second implementations that were described are based on a simple 2-terms linear approximation for the calculation of the time intervals φ_m and φ_{m+1}. This is not restrictive. Other approximations can be used. For instance a linear approximation using more than 2 terms can be used. The LMS updating scheme for these other approximations can be derived in a similar fashion as for the 2-terms linear approximation.
- The minimization algorithm used in the above described implementations is the LMS algorithm. This is not restrictive. Other minimization algorithm can be used to minimize Z_m. The corresponding coefficient updating equations would be derived easily by using the same principles as those described above for the LMS algorithm.
- In the cross-talk cancellation means described with reference to figure 5, the main signal is equalized. In an alternative embodiment the main signal could be processed by an adaptive filter in a similar fashion as the lower and upper satellite signal.

The functions described above may be implemented either in hardware or in software. Figures 1, 2 and 5 are functional representations of an apparatus and a signal processor according to the invention. A hardware implementation of same may differ from this functional block representation.

The word "comprising" doesn't exclude the presence of other elements or steps than those listed.

CLAIMS

1. A cross-talk cancellation method using a main signal (62) associated to a target track (32) and satellite signals (61, 63) associated to side tracks (31, 33), said main signal showing transitions (X_m) and runs of various lengths ($d_{m+1,m}$) between two transitions (X_m , X_{m+1}), said cancellation method comprising the steps of:
- filtering said satellite signals with adaptive filters (71, 73) thereby generating filtered versions (81, 83) of said satellite signals,
- updating the coefficients of said adaptive filters by minimizing the mismatch between the actual and the expected run length between two transitions of the main signal,
- processing said main signal thereby generating an improved main signal (102), said processing including a subtraction of said filtered versions of said satellite signals.

2. A program comprising instructions for implementing a cross-talk cancellation method as claimed in claim 1 when said program is executed by a processor.

3. A signal processor (40) comprising cross-talk cancellation means (42) for receiving a main signal (62) associated to a target track (32) and satellite signals (61, 63) associated to side tracks (31, 33), said main signal showing transitions (X_m) and runs of various lengths ($d_{m+1,m}$) between two transitions (X_m , X_{m+1}), said cross-talk cancellation means comprising:
- filtering means (71, 73) for filtering said satellite signals with adaptive filters thereby generating filtered versions (81, 83) of said satellite signals,
- updating means (111, 113) for updating the coefficients of said adaptive filters by minimizing the mismatch between the actual ($d_{m+1,m}$) and the expected ($d^{(exp)}_{m+1,m}$) run length between two transitions of the main signal,
- processing means (93) for generating an improved main signal (102) from said main signal by subtraction of said filtered versions of the satellite signals.

4. A signal processor as claimed in claim 3, comprising a fixed clock (55), time recovery means (130), and a bit clock (120) driven by said time recovery means, said fixed clock being asynchronous with respect to said bit clock, wherein said cross-talk cancellation means are operated at said fixed clock.

5. A signal processor as claimed in claim 4, wherein said bit clock has a bit clock frequency and said fixed clock has a fixed clock frequency that is substantially different from said bit clock frequency so that the ratio between said bit clock frequency and said fixed clock frequency is substantially different from 1, said signal processor further comprising time recovery means (50-

1, 50-2) for estimating said ratio and providing said ratio to said updating means, said updating means being designed to take said ratio into account for updating said coefficients.

6. An apparatus (6-1, 6-2) for reading a signal stored along a track on a storage medium (1) comprising a signal processor as claimed in claim 3.

7. An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 4.

8. An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 5.

ABSTRACT

CROSS-TALK CANCELLATION SCHEME FOR RLL-BASED STORAGE SYSTEMS

The invention applies to RLL-based storage systems. In modern storage systems, the inter-track spacing is chosen relatively small to allow for high storage densities. As a result, when reading a target track, data written on side tracks may appear in the recovered signal. This inter-tracks interference is called cross-talk.

The invention proposes a cross-talk cancellation scheme based on the minimization of the mismatch between the actual and the expected run length between two transitions of the signal. The proposed solution significantly improves the ramp-up properties of the receiver and allows more efficient hardware implementation.

Reference: figure 5

Application: optical storage, magnetic storage, magneto-optical storage.

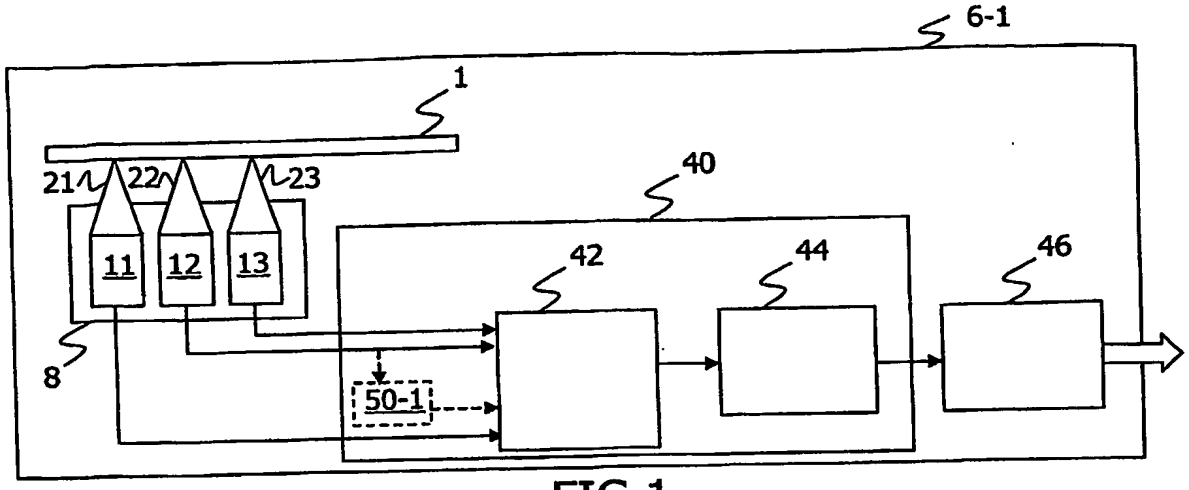


FIG.1

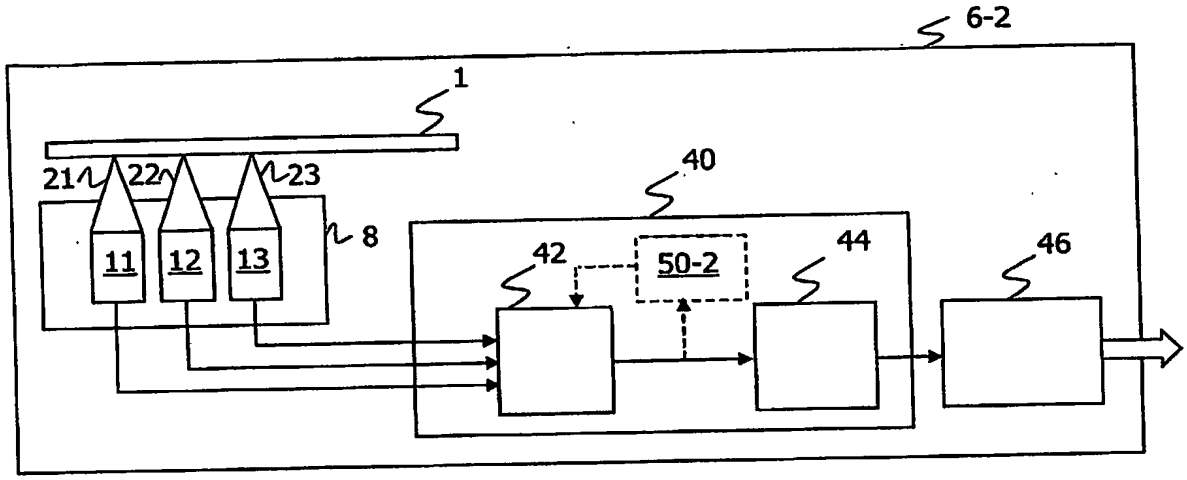


FIG.2

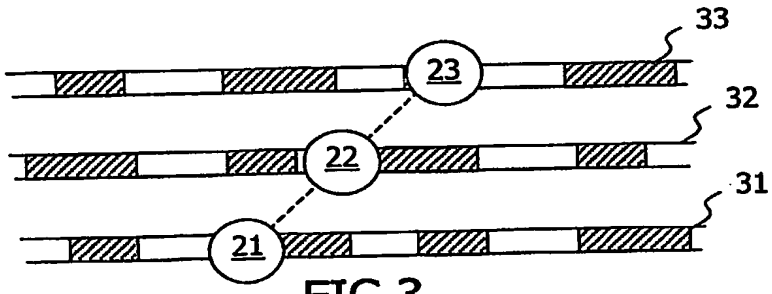


FIG.3

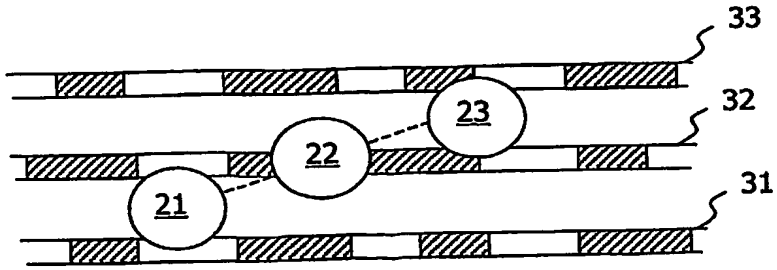


FIG.4

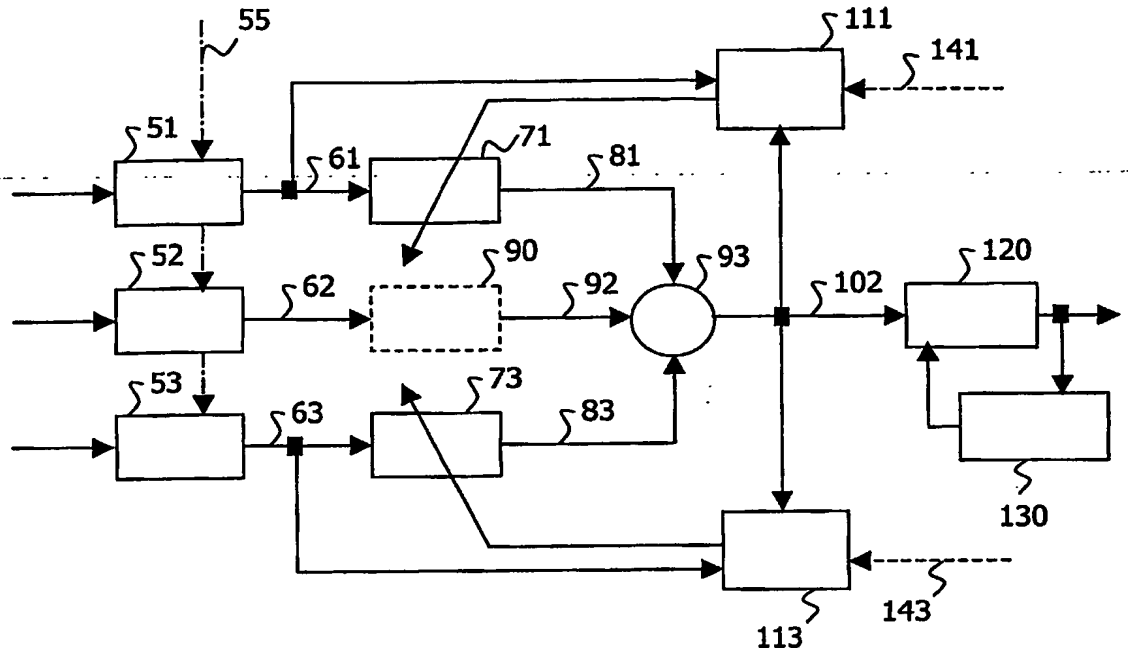

55
111
141
51
61
71
81
52
90
93
120
62
92
102
53
73
63
83
130
113
143

FIG.5

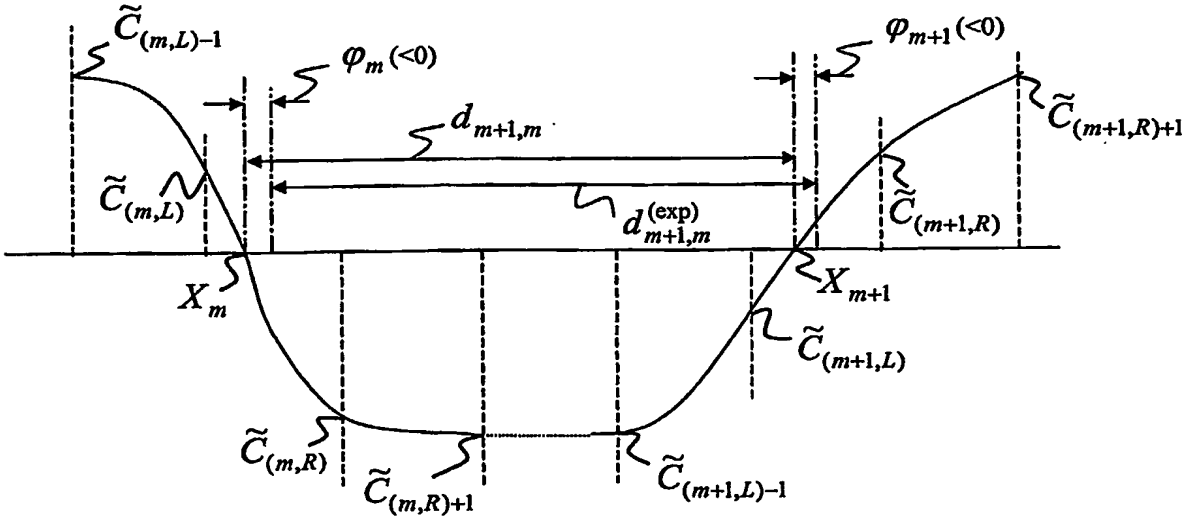
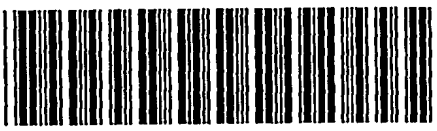

$\tilde{C}_{(m,L)-1}$
$\varphi_m (<0)$
$\varphi_{m+1} (<0)$
$d_{m+1,m}$
$\tilde{C}_{(m+1,R)+1}$
$\tilde{C}_{(m,L)}$
$d^{(exp)}_{m+1,m}$
$\tilde{C}_{(m+1,R)}$
X_m
X_{m+1}
$\tilde{C}_{(m+1,L)}$
$\tilde{C}_{(m,R)}$
$\tilde{C}_{(m,R)+1}$
$\tilde{C}_{(m+1,L)-1}$

FIG.6



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